NORMALLY-OFF POWER JFET AND MANUFACTURING METHOD THEREOF

CROSS-REFERENCE TO RELATED APPLICATIONS

The disclosure of Japanese Patent Application No. 2011-19438 filed on Feb. 1, 2011 including the specification, drawings and abstract is incorporated herein by reference in its entirety.

BACKGROUND

The present invention relates to a technology which is effective when applied to a device formation technique in a semiconductor device (or semiconductor integrated circuit device) and a manufacturing method thereof, i.e., particularly in a normally-off power JEFT and a manufacturing method thereof.

Japanese Unexamined Patent Publication No. 2008-66619 (Patent Document 1) discloses a Multi-Epitaxy technique in which, as a manufacturing process of a Normally-ON JFET (Junction Field Effect Transistor), epitaxial growth and ion implantation into portions serving as gates are repeated several times, and then activation annealing is simultaneously performed.

RELATED ART DOCUMENT

Patent Document

[Patent Document 1]
Japanese Unexamined Patent Publication No. 2008-66619

SUMMARY

In general, in a semiconductor active element such as a Normally-OFF JFET based on SiC in which an impurity diffusion speed is significantly lower than in silicon, trenches are formed in gate regions, and ion implantation into the side walls thereof or the like is performed to form the gate regions. However, the study conducted by the present inventors on such an element has revealed that there are problems as shown below. That is, for example,

(1) To ensure the performance of a JFET, it is necessary to control the area between the gate regions thereof with high precision.

(2) Since each of the gate regions is formed in a source region under process constraints, a heavily doped PN junction is formed between the source region and the gate region so that an increase in junction current cannot be avoided.

(3) Particularly high-energy ion implantation is required for edge termination.

(4) Since it is difficult to achieve electrode wiring immediately above the gate region, the gate resistance increases.

The present invention has been achieved to solve such problems.

An object of the present invention is to provide structure of a semiconductor device such as a highly reliable SiC-based JFET and a manufacturing process thereof.

The above and other objects and novel features of the present invention will become apparent from a statement in the present specification and the accompanying drawings.

The following is a brief description of the outline of a representative embodiment of the invention disclosed in the present application.

That is, an aspect of the present invention is a normally-off power JFET and a manufacturing method thereof and, according to a multi-epitaxial method which repeats a process including epitaxial growth, ion implantation, and activation annealing a plurality of times, a gate region including a plurality of areas is formed.

The following is a brief description of an effect obtained according to the representative embodiment of the invention disclosed in the present application.

That is, in a normally-off power JFET and a manufacturing method thereof, according to a multi-epitaxial method which repeats a process including epitaxial growth, ion implantation, and activation annealing a plurality of times, a gate region including a plurality of areas is formed. This allows high-precision setting of a gate-to-gate spacing.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a chip top view of an example of a target device in a manufacturing method of a normally-off power JFET of an embodiment of the present invention;

FIG. **2** is a schematic device cross-sectional view substantially corresponding to the X-X' cross section of a cut-away region R1 of the cell portion and peripheral portion of FIG. **1** (or FIG. **24**);

FIG. **3** is a wafer top view showing relations among a two-dimensional structure of a SiC wafer used in the manufacturing method of the normally-off power JFET of the embodiment of the present invention, a chip region corresponding to the chip of FIG. **1**, and the crystal orientation of the wafer;

FIG. **4** is a device cross-sectional view corresponding to FIG. **2**, which is for illustrating a main process (lithographic step for introducing a lower-layer P+ edge termination area) in the manufacturing method of the normally-off power JFET of the embodiment of the present invention;

FIG. **5** is a device cross-sectional view corresponding to FIG. **2**, which is for illustrating the main process (ion implantation step for introducing the lower-layer P+ edge termination area) in the manufacturing method of the normally-off power JFET of the embodiment of the present invention;

FIG. **6** is a device cross-sectional view corresponding to FIG. **2**, which is for illustrating the main process (ion implantation step for introducing lower-layer P+ gate regions) in the manufacturing method of the normally-off power JFET of the embodiment of the present invention;

FIG. **7** is a device cross-sectional view corresponding to FIG. **2**, which is for illustrating the main process (first activation annealing step) in the manufacturing method of the normally-off power JFET of the embodiment of the present invention;

FIG. **8** is a device cross-sectional view corresponding to FIG. **2**, which is for illustrating the main process (ion implantation step for introducing a middle-layer P+ edge termination area) in the manufacturing method of the normally-off power JFET of the embodiment of the present invention;

FIG. **9** is a device cross-sectional view corresponding to FIG. **2**, which is for illustrating the main process (ion implantation step for introducing middle-layer P+ gate regions) in the manufacturing method of the normally-off power JFET of the embodiment of the present invention;

FIG. **10** is a device cross-sectional view corresponding to FIG. **2**, which is for illustrating the main process (second